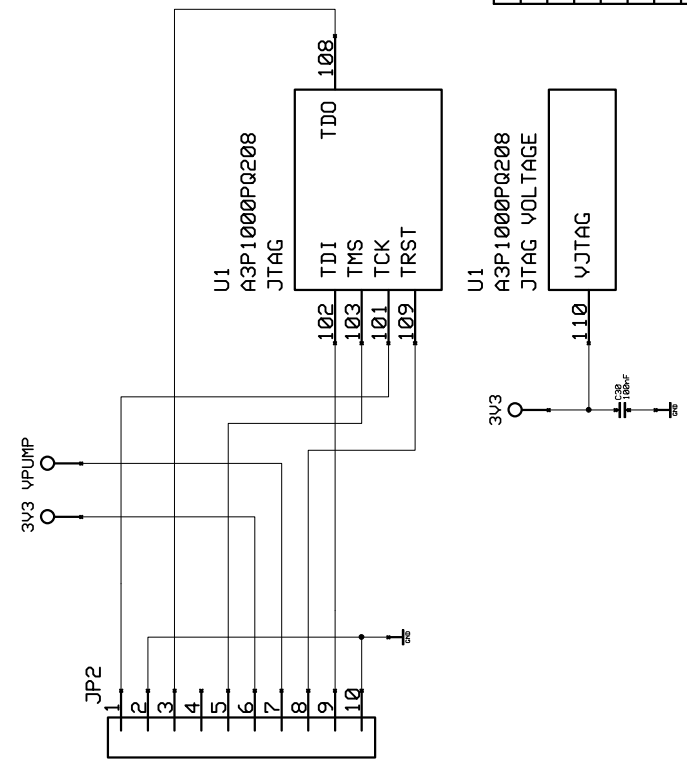
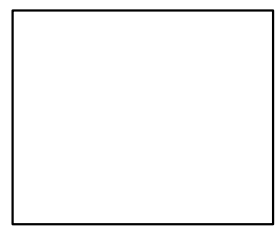


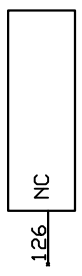
JTAG config



FPGAPWR

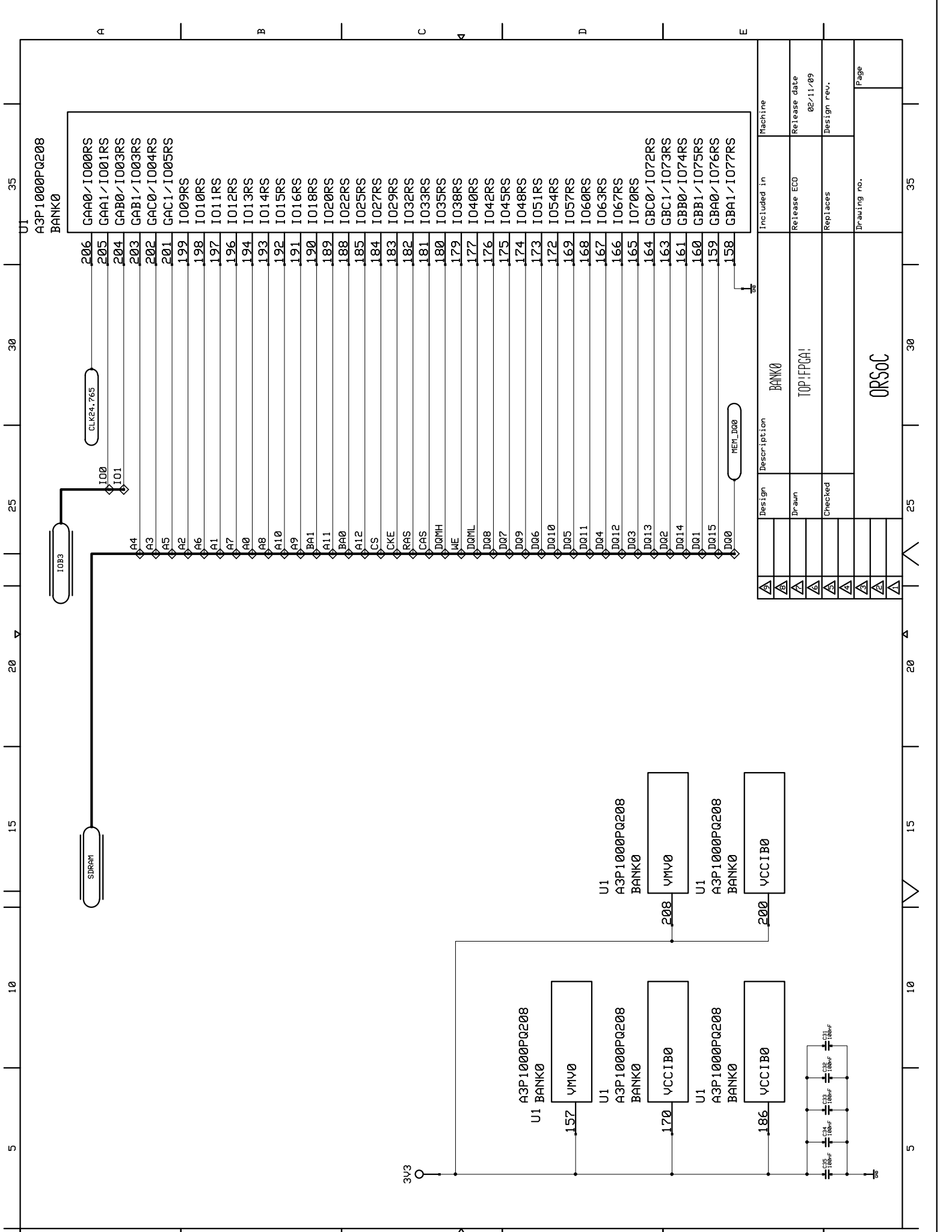


U1
A3P1000PQ208
NC



Design	Description	Included in	Machine
Drawn	FPGA	Release ECO	Release date
Checked	TOP!	Replaces	02/11/09
		Drawing no.	Design rev.
			Page

ORSoc



A3P1000PQ208 BANK0

206	GAA0/I000RS
205	GAA1/I001RS
204	GAB0/I003RS
203	GAB1/I003RS
202	GAC0/I004RS
201	GAC1/I005RS
199	I009RS
198	I010RS
197	I011RS
196	I012RS
194	I013RS
193	I014RS
192	I015RS
191	I016RS
190	I018RS
189	I020RS
188	I022RS
185	I025RS
184	I027RS
183	I029RS
182	I032RS
181	I033RS
180	I035RS
179	I038RS
177	I040RS
176	I042RS
175	I045RS
174	I048RS
173	I051RS
172	I054RS
169	I057RS
168	I060RS
167	I063RS
166	I067RS
165	I070RS
164	GBC0/I072RS
163	GBC1/I073RS
161	GBB0/I074RS
160	GBB1/I075RS
159	GBA0/I076RS
158	GBA1/I077RS

Design		Included in	Machine
Drawn	BANK0	Release ECO	Release date
Checked	TOP:FPGA1	Replaces	02/11/09
		Replaces	Design rev.
		Drawing no.	Page
	ORSoc		35

3V3

A3P1000PQ208
U1 BANK0

VMV0

A3P1000PQ208
U1 BANK0

VCCIB0

A3P1000PQ208
U1 BANK0

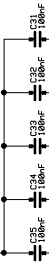
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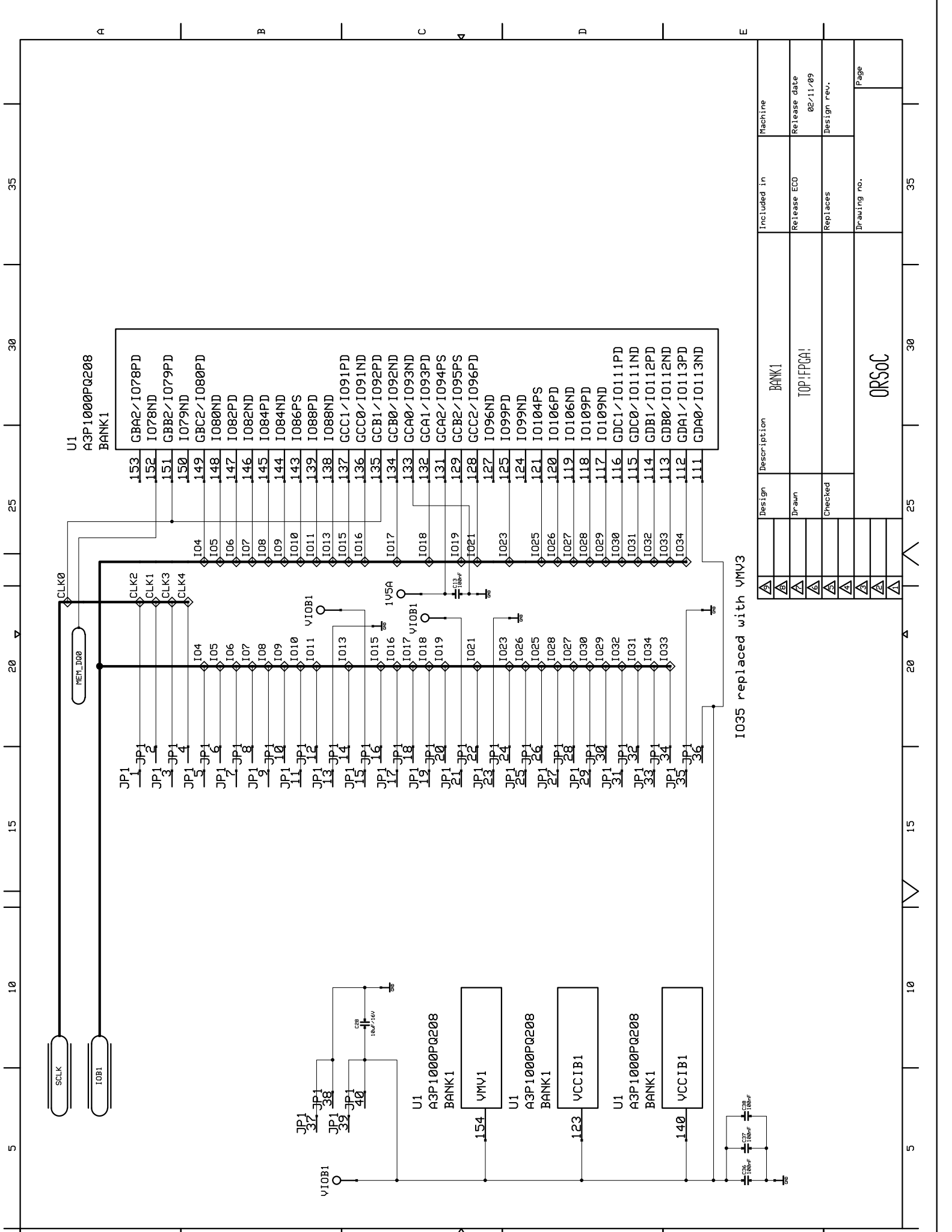
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A3P1000PQ208
BANK0

VMV0

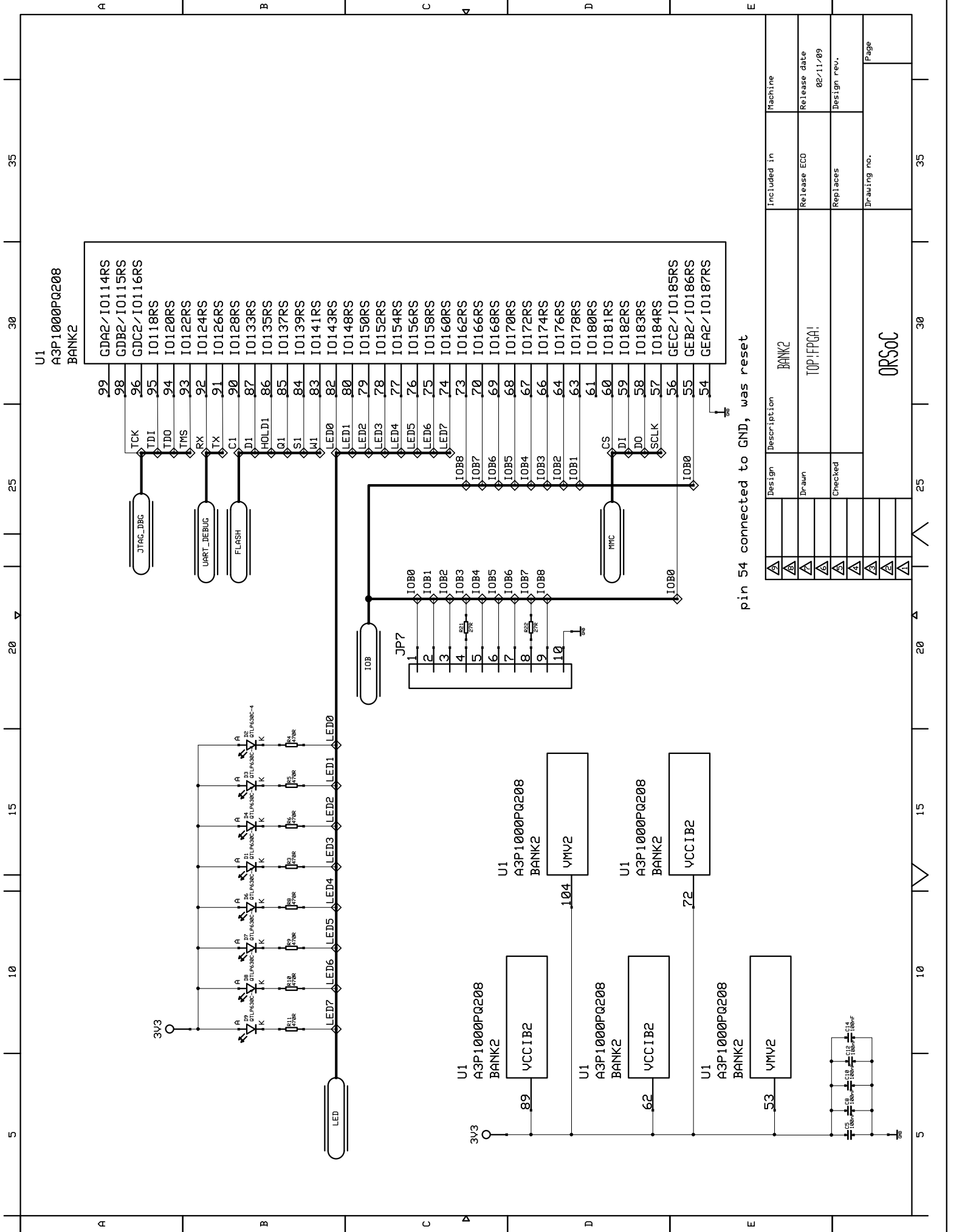
U1
A3P1000PQ208
BANK0

VCCIB0



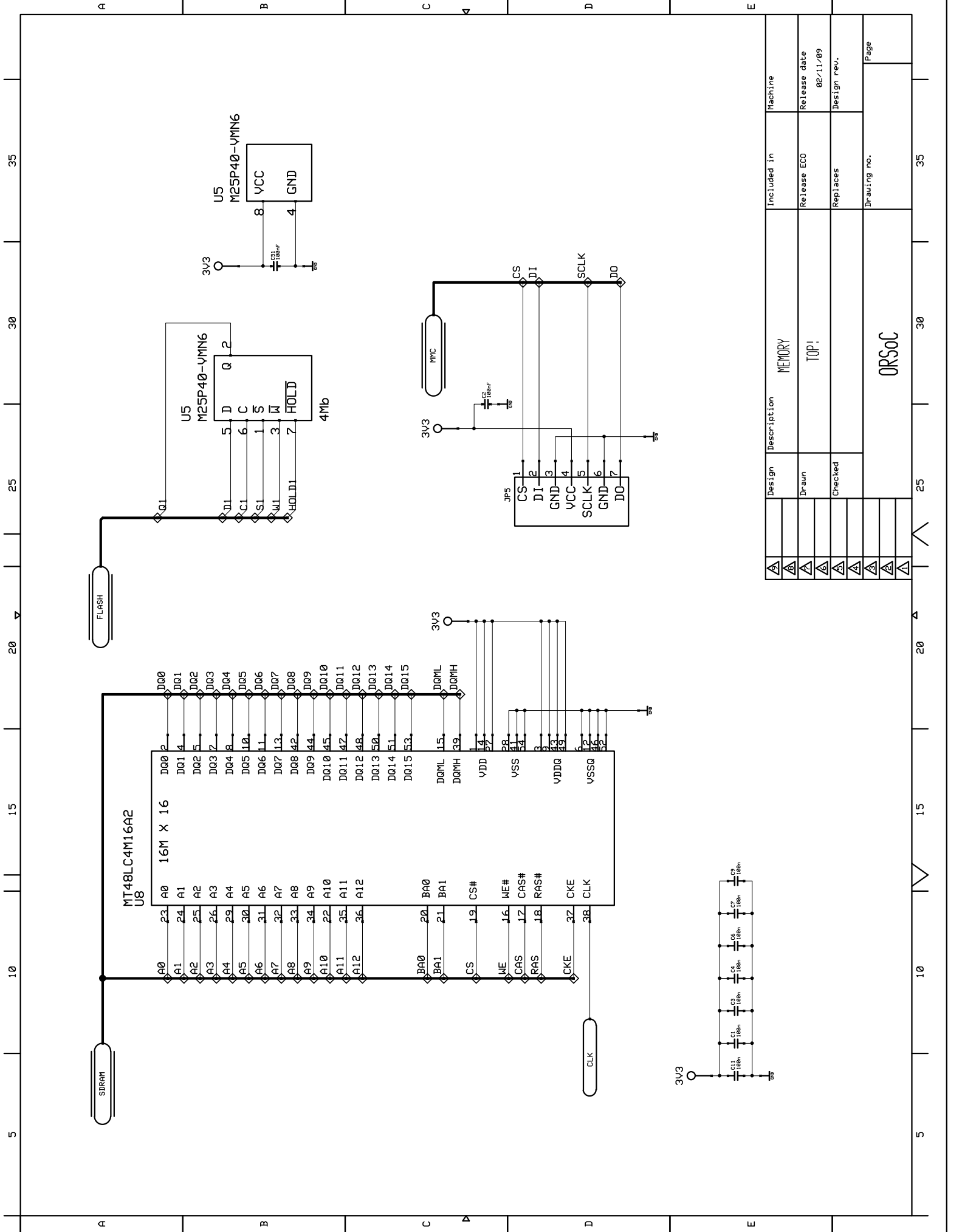


Design	Description	Included in	Machine
Design	BANK1	Release ECO	Release date
Drawn	TOP:FFPGA:	Replaces	02/11/09
Checked		Drawing no.	Design rev.
			Page



pin 54 connected to GND, was reset

Design	Description	Included in	Machine
▲	BANK2	Release ECO	Release date
▲	TOP:FPGA1	Replaces	02/11/09
▲		Drawing no.	Design rev.
▲	OR50C		Page



Design	Description	Included in	Machine
Drawn	MEMORY	Release ECO	Release date
Checked	TOP!	Replaces	02/11/09
		Drawing no.	Design rev.
			Page

